DESIGN AND EVALUATION OF AN HPVM-BASED WINDOWS NT SUPERCOMPUTER

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Summary

We describe the design and evaluation of a 192-processor Windows NT cluster for high performance computing based on the High Performance Virtual Machine (HPVM) communication suite. While other clusters have been described in the literature, building a 58 GFlop/s NT cluster to be used as a general-purpose production machine for NCSA required solving new problems. The HPVM software meets the challenges represented by the large number of processors, the peculiarities of the NT operating system, the need for a production-strength job submission facility, and the requirement for mainstream programming interfaces. First, HPVM provides users with a collection of standard APIs like MPI, Shmem, Global Arrays with supercomputer class performance (13 μs minimum latency, 84 MB/s peak bandwidth for MPI), efficiently delivering Myrinet's hardware performance to application programs. Second, HPVM provides cluster management and scheduling (through integration with Platform Computing's LSF). Finally, HPVM addresses Windows NT's remote access problem, providing convenient remote access and job control (through a graphical Java-applet front-end). Given the production nature of the cluster, the performance characterization is largely based on a sample of the NCSA scientific applications the machine will be running. The side-by-side comparison with other present-generation NCSA supercomputers shows the cluster to be within a factor of 2 to 4 of the SGI Origin 2000 and Cray T3E performance at a fraction of the cost. The inherent scalability of the cluster design produces a comparable or better speedup than the Origin 2000 despite a limitation in the HPVM flow control mechanism.

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1 Introduction

The advent of "killer micros" and "killer networks" is enabling clustered commodity machines to compete with supercomputers in aggregate performance. Many supercomputers today are microprocessor-based (Silicon Graphics, 1996; Scott, 1996; IBM, 1995; Cray Research, 1993; Sun Microsystems, 1997) because such microprocessors deliver instruction and floating point processing rates in excess of 1 billion operations per second. In addition, emerging high-speed networks (American National Standards Institute, 1987) provide the aggregate capability for supercomputing performance. While the development of these technologies has long been anticipated, their potential impact has been accentuated by the development of new communication technology described below.

Over the past 4 years, the research community has produced dramatic progress in delivering hardware communication performance to applications (Fast Messages [FM] [Pakin, Karamcheti, and Chien, 1997]; Active Messages [AM] [Chun, Mainwaring, and Culler, 1997]; U-Net [von Eicken et al., 1995]; VMMC-2 [Dubnicki et al., 1997]; PM [Tezuka, Hori, and Ishikawa, 1996]; BIP [Prylli and Tourancheau, 1997]; MINI [Hady, Minnich, and Burns, 1994]; and Osiris [Druschel, Peterson, and Davie, 1994]). These efforts have forged a consensus on core requirements for network interfaces to deliver high communication performance to application programs. This consensus includes the following key features, which have recently been incorporated in the Intel/Compaq/Microsoft standard for cluster interfaces—the Virtual Interface Architecture (1997a).

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- user-level protected network access,
- hardware support for gather-scatter,
- early demultiplexing of incoming traffic, and
- lightweight protocols.

Challenges to building a large cluster, particularly one based on PCs and Windows NT include system selection, integration, delivering communication performance, cluster scheduling and management, and remote access. Our cluster is based on technology from the High Performance Virtual Machines (HPVM) project,[1] which provides

- High Performance Communication: 10 μs latency and 90 MB/s bandwidth employing *Fast Messages* to implement MPI, Global Arrays, Shmem Put/get
- Management and Scheduling: Flexible scheduling, system monitoring, and job monitoring using Platform Computing's Load Sharing Facility
- Remote Access: Job submission, monitoring, and control of jobs via a Java applet front-end, which runs on any Java-enabled system

Using these technologies, we built a 192-processor cluster, employing dual-processor 300 MHz Pentium II PCs and 160 MB/s Myrinet. The resulting 58 GFlops system has 45 GB of DRAM, 1.6 GB/s of bisection bandwidth, and 400 GB of disk storage. The cluster is a National Computational Science Alliance (NCSA) project built in collaboration by the Concurrent Systems Architecture Group (CSAG) and the NCSA. It was integrated in 6 weeks, though it exploited a much longer chain of technology developed in FM and HPVM, and was demonstrated at the Alliance '98 meeting on April 27, 1998. It went into production at NCSA in fall 1998 in time to be demonstrated at Supercomputing '98: at the Alliance booth, the NT cluster located in Urbana was used to perform simulations of Einstein's general relativity theory using Cactus and to perform two-dimensional Navier Stokes calculations using AS-PCG achieving 6.9 Gflops on 128 of the processors. Because of the success of the project, a follow-on cluster of 512 processors is planned for late 1999.

Several aspects set apart this cluster from a number of similar projects. The first is the use of Microsoft Windows NT 4.0[2], an operating system with 30 million installed units but not traditionally associated with high performance computing and clusters. The second is the scalability analysis of a complete stack of communication software layers (from the network interface card firmware all the way up to MPI) over a two-orders-of-magnitude range in the number of processors and machines (1 to 192, 1 to 96, respectively). Finally, the cluster was built to serve as a general-purpose production machine in a national supercomputing center rather than a research prototype, targeting high-end applications with floating point performance, core memory, and bisection bandwidth requirements in excess of, respectively, 10 Gflops, 10 GB RAM, and 1 GB/s.

We pioneered the use of Windows NT because we sought to extend the notion of commodity cluster to the software environment seen by the users. None of the other inexpensive commodity operating systems available for the Intel platform can compete with NTs abundance of tools and applications, degree of industrial acceptance, and amount of investments for support and development. And most important, the pervasiveness of the Windows user interface eases familiarization and acceptance by new users. We believe this to be a relevant concern as clusters of PC are putting high performance computing within reach of new scores of industrial and commercial users.

The contributions of this paper include lessons learned from building and evaluating such a large cluster.

First, the use of the cluster as a production machine required that adequate cluster management and scheduling functionalities had to be built on top of NT. This task was complicated by the desktop-centric nature of NT. By integrating a commercial-strength product like Platform Computing's LSF into HPVM, we were able to achieve the advanced level of service required with a modest effort. Over the course of a long and productive interaction with the HPVM team, Platform Computing accrued parallel job management services on top of LSF's native distributed computing concept.

Second, building the cluster exposed a wealth of software scaling issues in the HPVM software, Platform Computing's LSF software, and the underlying Windows NT operating system software. Many of these have been patched, some have been permanently fixed, but all of these are documented in this paper.

Third, the performance of the cluster itself is interesting, both microscopically and macroscopically, and we study and document the performance of the overall system both on microbenchmarks and on a sample of the cluster's planned workload of scientific applications. Depending on the application, the cluster is within a factor of 2 to 4 from SGI Origin 2000 and Cray T3E performance, with overall comparable or better scalability. While

achieving comparable absolute performance will require Intel processors to become twice as fast in terms of floating point performance, the cluster is already at an advantage in terms of price/performance.

Finally, the intention of the authors, as well as of both the HPVM project and NCSA, is to disseminate knowledge about building similar clusters, and thus we describe our experience in building the cluster—problems, snafus, and gotchas.

The rest of the paper is organized as follows. Section 2 describes the background technologies that are exploited in the HPVM cluster. In Section 3, the hardware and software in the cluster are described in detail. Basic system microbenchmarks and related performance figures are found in Section 4. Cluster performance on application programs is also presented in Section 4. Section 5 analyzes the results and discusses our experience in building the cluster. Finally, Section 7 concludes the paper and presents the future developments in progress.

"We pioneered the use of Windows NT because we sought to extend the notion of commodity cluster to the software environment seen by the users."

2 Background

Commodity cluster computing has been an active area of research since well before the advent of high performance interconnects. There is an obvious trade-off between application granularity and communication performance, on one side, and between communication performance and cost, on the other side. Different approaches to cluster computing have explored different segments along the axes of cost and of degree of generality.

The idea of tapping unused CPU cycles on networked machines is at the base of idle cycle scavenging systems such as Condor (Litzkow, Livny, and Mutka, 1988) and Legion (Lewis and Grimshaw, 1995). These systems transparently schedule applications, or application components, on machines detected to be in an idle state. In these kinds of systems, application execution is subjected to available space/available time constraint in exchange for a zero-cost source of computing power.

The simultaneous reduction in PC price and increase in x86 processor performance turned the notion of dedicated clusters into something economically feasible. The reliance of Beowulf clusters (Becker et al., 1995) on basic, well-established Fast Ethernet technology represents the lowest cost version of the dedicated cluster approach. By embracing the use of legacy protocols with their inherent latency/bandwidth limitations, the Beowulf approach is better suited to large-grained applications. The Beowulf concept emphasizes performance/price ratio over generality of use.

The advent of fast interconnect technologies (American National Standards Institute, 1987; Anderson and Cornelius, 1992; Boden et al., 1995; Garcia and Watson, 1997; IEEE Std., 1993) has changed the role of cluster architectures—from machines for coarse granularity applications to inexpensive general purpose parallel computers. A substantial amount of research efforts have been directed at the problem of delivering communication performance to applications (FM [Pakin, Karamcheti, and Chien, 1997]; AM [Chun, Mainwaring, and Culler, 1997]; U-Net [von Eicken et al., 1995]; VMMC-2 [Dubnicki et al., 1997]; PM [Tezuka, Hori, and Ishikawa, 1996]; BIP [Prylli and Tourancheau, 1997]; MINI [Hady, Minnich, and Burns, 1994]; and Osiris [Druschel, Peterson, and Davie, 1994]).

Some of these and other efforts have also produced large-scale clusters. In the Berkeley NOW project cluster, a Myrinet interconnect links together 104 Ultra SPARC workstations running communication software based on AM (http://now.cs.berkeley.edu). The Real World Computing Partnership's PM effort has produced the PC Cluster II consisting of 64 (128 since Spring 1998) 200 MHz Pentium Pro interconnected by a Myrinet network and running Linux (http://www.rwcp.or.jp/home-E.html). In the Netherlands, the DAS initiative links clusters in four universities with a ATM WAN as a research testbed for parallel programming and wide area distributed computing; the larger cluster at the Vrije Universiteit of Amsterdam is built of 128 200 MHz Pentium Pro interconnected by a Myrinet network and running BSD/OS (http://www.cs.vu.nl/~bal/das.html).

The HPVM research project has focused on crucial aspects of the design of high performance messaging layers such as the trade-offs between protocol processing overhead and the functionalities exposed in the programming interface. The key design decisions taken for the original FM (Pakin, Lauria, and Chien, 1995) implementation provided key communication services while retaining microsecond-level overhead, and over the course of two more releases led to the present 9 μs minimum latency and 92 MB/s peak bandwidth of HPVM. Since its first release in spring 1995, FM has been used in numerous other research projects exploring different areas of high performance communication. The implementation of the higher-level APIs on top of FM (MPI [Lauria and Chien, 1997]; Global Arrays, Shmem [Giannini and Chien, 1998]) turned into a study on efficient software layering (Lauria, Pakin, and Chien, 1998). FM has been used as a testbed for research on novel mechanisms for coscheduling on a network of workstations (Sobalvarro et al., 1998) and on the introduction of quality-of-service (QoS) guarantees in a wormhole routing interconnect (Connelly and Chien, 1997). HPVM is available for download on our Web site at http://www-csag.ucsd.edu.

3 The Machine: HPVM III

Cluster Software. The software is based on the Illinois HPVM technology, which includes Illinois FM^3 (Pakin, Lauria, and Chien, 1995) to deliver high bandwidth (92 MB/s) with low overhead (a few μs), and low latency (< 9 μs), achieving a half-power message size of 250 bytes while providing reliable and in-order delivery, and flow control.

HPVM also includes efficient implementations of standard scientific computing APIs (MPI [Lauria and Chien, 1997; Lauria, Pakin, and Chien, 1998]; Global Arrays, Shmem [Giannini and Chien,1998]) atop FM. Performance highlights include 13.3 μs minimum latency and 84.2 MB/s peak bandwidth for MPI-FM, 14.4 μs minimum latency and 76 MB/s peak bandwidth for a Shmem's shmem_put operation. These APIs enable the easy porting and the high performance required to integrate the existing NCSA scientific applications in the cluster environment.

HPVM provides basic cluster monitoring and scheduling by integrating Platform Computing's Load-Sharing Facility (Zhou et al., 1993) and adding a Java front-end for convenient remote access from any platform supporting a Java-enabled browser (Figure 1(a)).

The main component of the front-end is an applet whose graphical interface displays the list of available hosts, queues, and currently enqueued jobs (the "HPVM client" window in Figure 1(b)). Through the menu bar, other applets can be started, each giving access to the LSF services providing user authentication, cluster monitoring, and job management. In Figure 1(b), the real-time monitor applet window is shown (the "HPVM Real-time Monitor" window), with the list of available node statistics visible in the upper half.

Cluster Hardware. HPVM III comprises 192 300 MHz Pentium II processors in 96 nodes (two-way SMPs), 48 GB of memory (512 MB per node), 384 GB of disk (4 GB per node), 160 MB/s full duplex Myrinet networking (per node), and 100 Megabit Ethernet. Each machine is running its copy of Windows NT 4 Server, with the Fast Ethernet being used for file system sharing and machine administration. The machines are also connected as shown in Figure 2 using a collection of Myrinet Octal-8 and Dual-8 switches. A fat-tree topology was chosen for

(a)

(b)

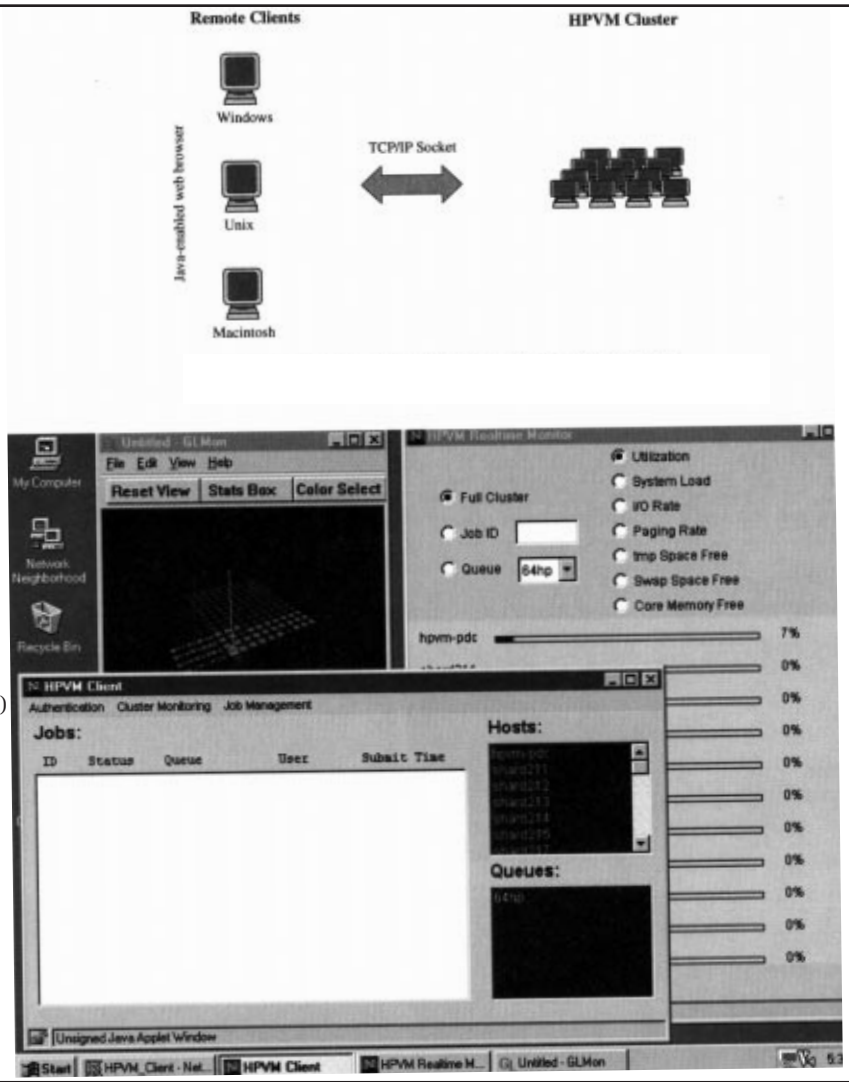

Fig. 1 The HPVM front-end
(a) The Java front-end enables access to the cluster from any Java-enabled browser.
(b) The HPVM front-end and real-time monitor applets. The real-time monitor statistics are also displayed in a 2D bargraph format by GLmon, a small graphical utility developed at NCSA (upper left).

being deadlock-free, readily expandable, and reasonably cost-effective, giving 1.62 GB/s of bisection bandwidth. The tree is organized in three levels of switches, the lowest one built of Myrinet octal switches, each connected directly to 16 nodes (each line in the figure is a dual-link cable). Given the low routing latency of Myrinet, we found the exact topology to be less critical than the bisection bandwidth or the balanced distribution of routes between switches (HPVM is statically routed).

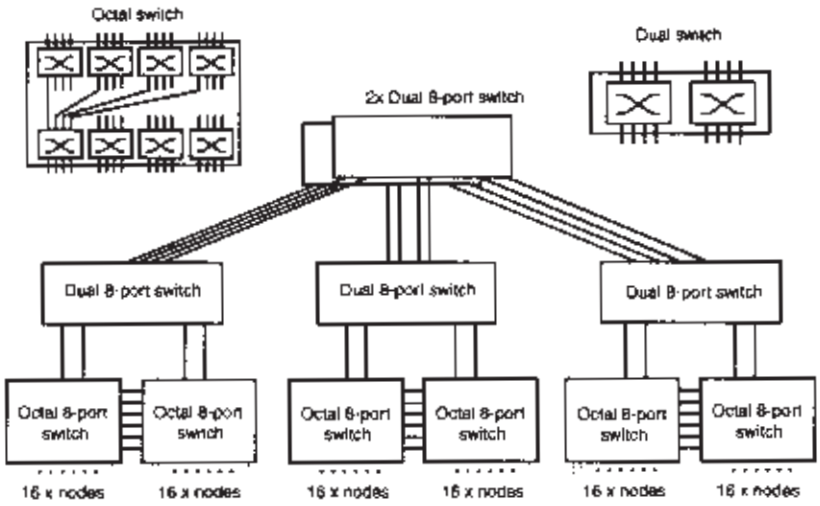

Fig. 2 The fat-tree cluster topology

The node type and configuration was determined by extensive testing of a wide range of machines (nine machines from five vendors), with a focus on evaluating I/O subsystem performance. Testing targeted the elements critical for communication performance, namely, memory bandwidth and I/O performance for both DMA and PIO transfers. The apparent homogeneity of PC hardware is illusory, with performance-varying factors of 2 or 3 across different vendors, motherboards, and configurations. For example, we observed variations of 44 to 108 MB/s memory-to-memory copy bandwidth.

We chose the Hewlett-Packard Kayak XU, a dual Pentium II 300 MHz model, as our cluster building block. This model sustained a single-CPU sustainable memory copy bandwidth of 108.4 MB/s, a DMA-In/DMA-Out peak bandwidth of 122.5/120.9 MB/s, and a PIO-Read/PIO-Write peak bandwidth of 10.6/132.2 MB/s. The detailed list of measurements for this and other machines is available on our Web site at http://www-csag.ucsd.edu/projects/comm/hcl.html.

The PCs occupy five meters of two-meter-high racking. The 96 machines require approximately 10 kW of power and cooling. Each keyboard, monitor, and mouse is shared by 16 machines through a Raritan console switch, resulting in a large saving on space, energy, cooling, and on the total cost. The console switch deals with Windows boot sequences, which require the presence of a keyboard

and allow access to each machine for system administration purposes.

Local disks are used for operating system, local paging, and temporary storage. We are planning a number of additional PCs to act as fileserver with enhanced storage performance and capability. A disk imaging utility is being employed to clone the configuration of a master and simplify the task of updating communication and system software.

4 Evaluation

4.1 MICROBENCHMARKS

Microbenchmarks were used to determine the peak communication performance and the basic limitations of HPVM. Microbenchmarks involve pairwise and multiparty communication.

Since HPVM is a cluster of SMPs, the microbenchmarks also explore the impact of different process placements (one or two per node). Critical issues here include memory, I/O bus, and NIC contention. All the benchmarks are performed through the MPI interface, using MPI_Send, MPI_Recv, and MPI_Barrier calls. Table 1 summarizes the results. These and the other results presented in this section have been measured at the end of April 1998.

"Microbenchmarks were used to determine the peak communication performance and the basic limitations of HPVM. . . . We used them to test and isolate the contribution to global performance of individual parts of the system such as flow control and the route allocation policies."

Latency. Latency was measured using the classical repeated ping-pong scheme; the result is the median value of a series of measurements. Figure 3 shows the latency for processes allocated both on two different nodes and on the same dual processor node. In the first variant, both nodes directly connected through an octal switch and nodes connected by multiple switches (> 4) have been considered.

The minimum latency for a 0-byte message between different nodes is 13.3 μs for nodes connected through one octal switch. An additional latency of less than 1 microsecond is seen between nodes connected through multiple switches. These numbers are comparable to those found on current generation supercomputers. For example, MPI minimum latency on the T3E is 14 μs (Anderson et al., 1997).

Process allocation makes a difference in latency. In the dual processor allocation, this is due mainly to the sharing of the I/O bus and of the LANai for both sending and receiving. This implies a lesser peak bandwidth (see next section), which explains the different slope of the two curves. Note that since bandwidth does not matter for very short messages, the two curves grow at the same rate

Table 1
Summary of MPI-FM Microbenchmark Results

Test	Performance
Point-to-point bandwidth	84.2 MB/s
Point-to-point latency	13.3 μs
Scaling point-to-point bandwidth	various, see Figure 4
192 party barrier	290 μs
Bisection bandwidth	1.62 GB/s

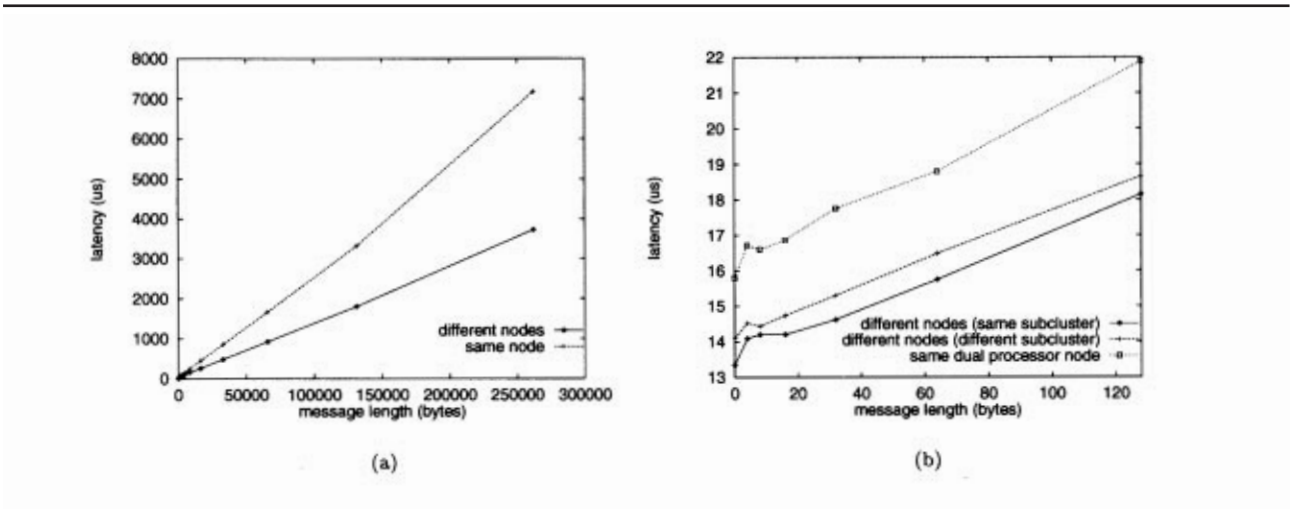

Fig. 3 Latency between two MPI processes
(a) long messages
(b) short messages

with a higher fixed cost when the dual processor allocation is used.

Bandwidth. Bandwidth was measured by sending a sequence of messages in a row and stopping the watch on the acknowledgment for the last one. The reported result is the median of several consecutive tests.

In Figure 4(a), bandwidth is shown both for processes allocated on two different nodes and on the same dual processor node. The peak bandwidth for the multiple node case is 84.2 MB/s for 128 Kbytes messages. The sharp decrease in bandwidth for messages longer than 128 Kbytes is due to cache effects in connection with the second-level cache. The half-performance message length $N_{1/2}$ is 970 bytes, which is less than half the FM packet size. The bandwidth for the dual processor case is lower as expected, since the I/O bus and the network interface are shared between the sender and the receiver. As a reference, the T3E peak bandwidth stands at 260 MB/s (Anderson et al., 1997).

Scaling Bandwidth. The credit-based flow control scheme of FM equally allocates an amount of credits to all processes of a computation. To evaluate the impact of static credit partitioning as the number of processes increases, we used a test similar to the bandwidth test, in which $N \geq 2$ processes are spawned instead of two. Process 0 and process 1 act as the sender and the receiver of a standard bandwidth test, while all the other processes are idle waiting for program termination.

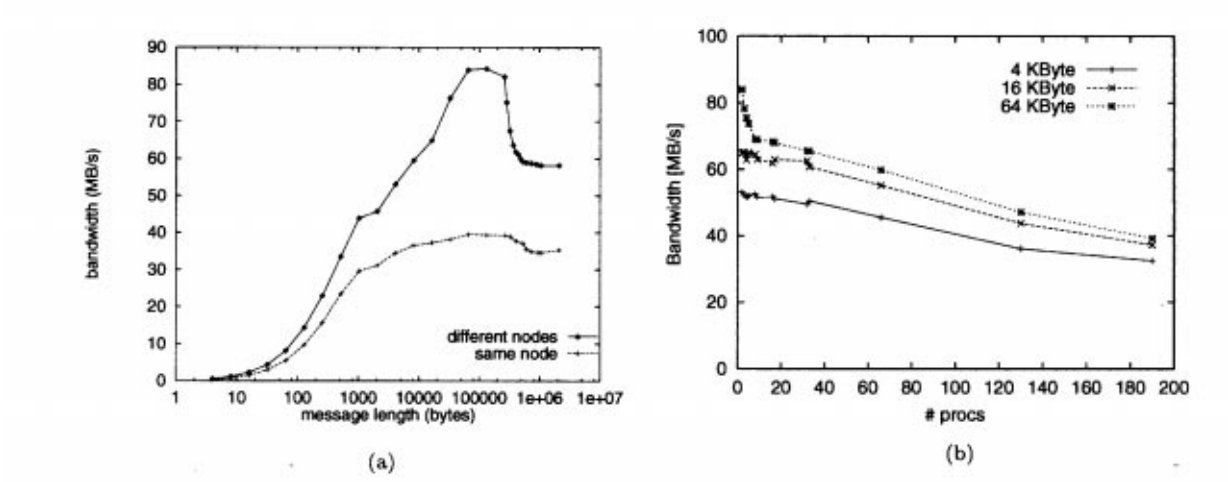

Fig. 4 MPI bandwidth
(a) bandwidth between two MPI processes
(b) dependence of bandwidth on the number of processes

Figure 4(b) shows how the bandwidth varies with the number of processes for a given message length. Peak bandwidth decreases by as much as 50% over the entire range as the number of processes increases. By statically allocating an equal number of credits to all processes, the scheme trades simplicity for efficiency in the buffer management. The impact on application performance will be discussed later in the paper.

Barrier. We measured the execution time of the MPI_Barrier operation as a function of the number of processes involved. The test, after a preliminary barrier to synchronize the processes, performs `num_reps` of barrier operations in a row.

In Figure 5(a), the barrier completion time is reported for two allocation schemes, one and two processes per node. In both cases, the curve increases logarithmically as expected. We observe a higher completion time when both the processors in each node are involved. This is likely due to contention on the I/O bus, which increases the gap between successive messages.

The absolute performance is remarkable, considering that, for example, on the Origin 2000 the barrier takes more than 1 ms to complete on 64 nodes (the T3E hardware-supported barrier completes in 7 μs on 256 nodes). If N is the number of processes involved, for single processor allocation the barrier completion time

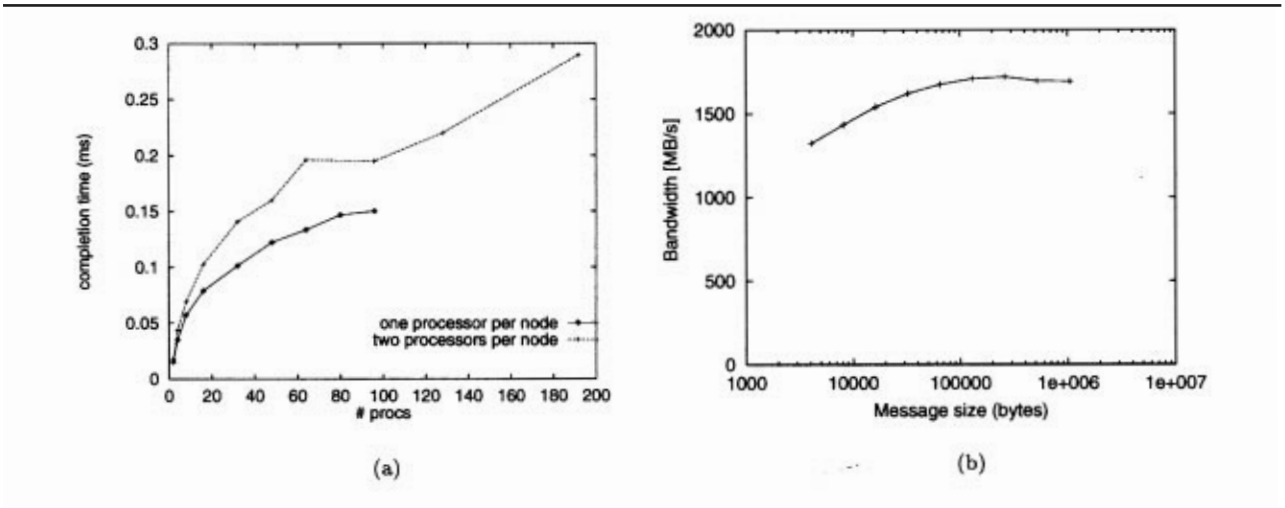

Fig. 5 Barrier and bisection bandwidth
(a) barrier completion time
(b) cluster bisection bandwidth

grows as 22 log N µs, while for dual processor allocation it grows as 31 log N µs.

Bisection Bandwidth. In this test, the bandwidth test is performed in parallel between $N/2$ pairs of processes allocated in such a way to saturate the bisection cut. The present peak value of 1.62 GB/s (Figure 5(b)) is the result of an improved route allocation policy and an upgraded interconnect with respect to the initial one used in the April '98 Alliance meeting. We doubled the top half of the tree to achieve a more balanced topology. This required modifying the HPVM static routing algorithm, based on an up*/down* scheme, to handle trees with more than one root. The up*/down* routing scheme (Schroeder et al., 1990) works by first computing a breadth-first logical tree starting from an arbitrary node (ideally the physical root in case of tree topology) and assigning an "up" and a "down" direction to each link in the network based on the computed tree. The scheme then mandates that all legal routes be composed of zero or more links in the "up" direction, followed by zero or more in the "down" direction. Such restriction prevents deadlock by avoiding the formation of dependency cycles between links. In our modified scheme, the "up" and "down" assignment is modified to accommodate multiple roots. The result is a balanced allocation of routes across the multiple trees; however, the use of more than one root makes the scheme potentially deadlock-prone in nontree topologies.

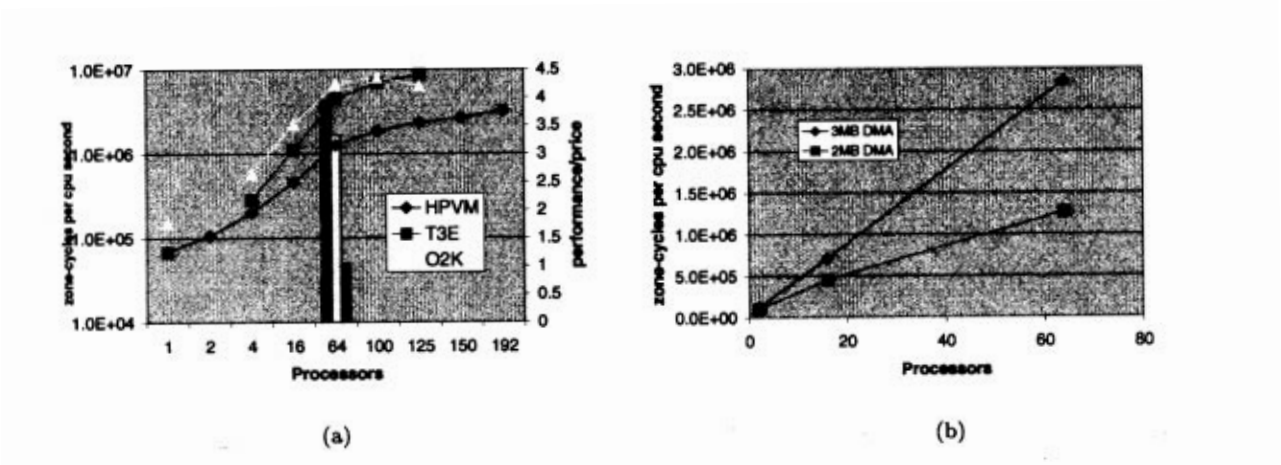

Fig. 6 ZeusMP performance
(a) comparison across machines
(b) the effect of a simple improvement in the flow control mechanism—a larger DMA kernel buffer

4.2 APPLICATIONS

We present the performance measurements of four applications taken during the Alliance '98 meeting and in the following months. These applications are also running on other NCSA supercomputers, allowing a direct comparative assessment of the system.

- ZeusMP (Fiedler, 1997) is a computational fluid dynamics code in Fortran using MPI developed at the Laboratory for Computational Astrophysics (University of Illinois at Urbana–Champaign) for the simulation of astrophysical phenomena. ZeusMP solves problems in three spatial dimensions with a wide variety of boundary conditions.
- Cactus. The Cactus code is a modular high performance 3D tool for numerical relativity. Cactus is developed jointly by researchers at AEI-Potsdam, NCSA, Washington University, and elsewhere.
- AS-PCG kernel. The AS-PCG is a preconditioned conjugate gradient method with an additive Schwarz-Richardson preconditioner for solving linear systems. It was developed by Danesh Tafti et al. at NCSA.
- QMC kernel. This is a quantum Monte Carlo simulation method developed by the NCSA Condensed Matter Physics group at NCSA, and it is being used to perform studies of electronic structure of molecular and condensed matter systems.

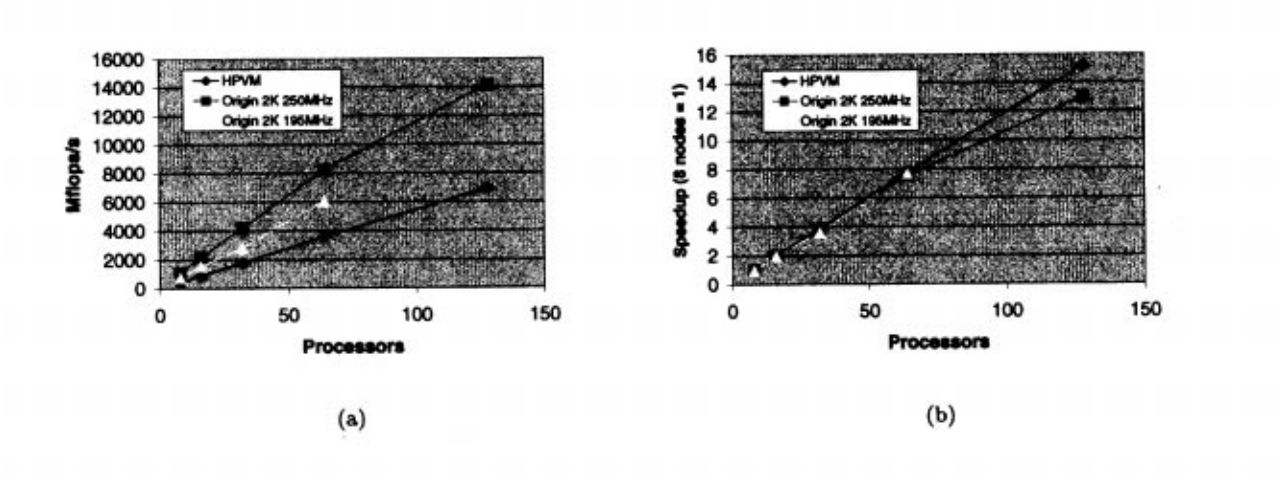

Fig. 7 AS-PCG performance
(a) absolute performance
(b) speedup

The applications encompass a wide range of computation granularity, with ZeusMP representing one extreme (low granularity) and Cactus the other. ZeusMP (Figure 6(a)) and AS-PCG (Figure 7) were instrumental in evaluating and contrasting scalability. (We could not use fewer than eight processors in the AS-PCG comparison because of memory limitations.) The other applications, Cactus and QMC (Figure 8) provide useful information on the comparative floating performance of the different architectures. All the applications are examples of preexisting scientific codes that required only a modest recompilation effort to run unmodified on the cluster. No particular tuning was performed on the new platform to get the results shown.

Depending on the application, performance is between a factor of 2 (AS-PCG) and of 4 (ZeusMP) lower than the Origin 2000 and the Cray T3E. With respect to the two coarse-grained applications, the factor for Cactus is 2.5 and for QMC is 1.8. Contrasting these values against the latency benchmark results, the conclusion is that the floating point performance of the nodes accounts for a large share of the performance gap. The baseline factor of 2 found in application performance is consistent, for example, with the SPECfp95 ratings of an Intel 300 MHz Pentium II motherboard and of the 195 MHz version of the Origin 2000, respectively, 8.82 and 19.2, as reported on the SPEC Web site (http://www.spec.org).

The additional factor of 2 seen in some applications is the effect of the reduced bandwidth produced by the flow

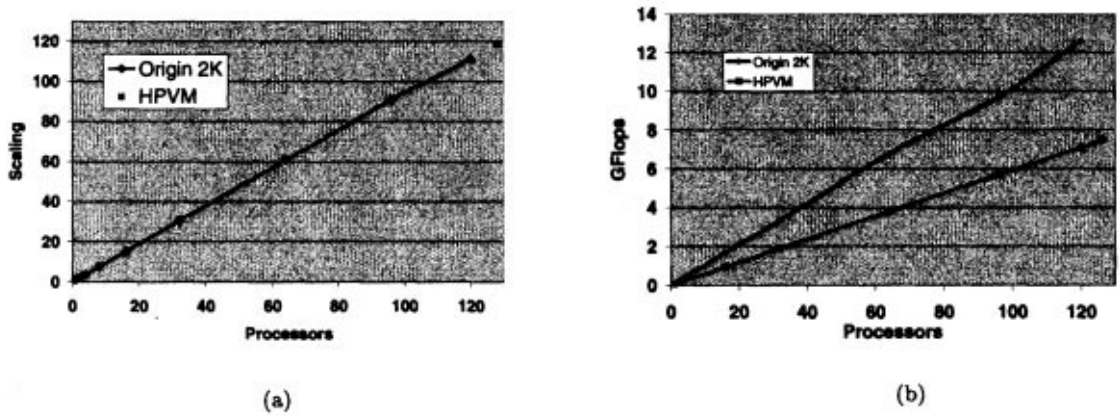

Fig. 8 Scaling of Cactus and QMC
(a) cactus
(b) QMC

control limitations on bandwidth intensive applications. We tested this effect using ZeusMP. The graph in Figure 6(b) shows that a 50% increment of the size of the kernel DMA region from the current value of 2 MB to 3 MB results in an approximate doubling of performance. The increase to 3 MB adds enough buffering to substantially flatten the bandwidth curve of Figure 4(b) given the current delays in the credit recirculation mechanism. Such value represents only a modest additional cost in absolute terms and less than 1% of the physical memory of the machines.

While extending the size of the DMA region is a practical solution for the short term, other solutions are under investigation. For example, we are testing some low-level optimizations aimed at increasing the efficiency of the credit circulation in the system and that are showing an improved flatness of the bandwidth graph of Figure 4(b) without additional buffering. In another approach, a dynamic credit allocation scheme that adapts to the effective level of communication activity has been proposed (Canonico, Cristaldi, and Iannello, 1999).

5 Discussion and Lessons

The cluster started working in mid-April, right after the last PC was plugged in. By using fully functional, proven-technology building blocks (PCs, Myrinet LAN, HPVM), we found ourselves comparing performances a

mere 6 weeks after opening the boxes of the last shipment of PCs. We learned a number of things in the process.

Given the focus of the project on programmability and standard interfaces, MPI-based applications happened to be among the first codes to run on the cluster. The effort of porting Unix applications to Windows NT was less than anticipated, with a number of annoying minor compiler incompatibilities taking center stage over differences in the runtime environments.

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Connected to the porting issue is the relatively scarce availability of optimized standard libraries for scientific computing under Windows NT. In porting some of the applications, we had to use our own build of the BLAS and LAPACK libraries, whereas highly optimized versions are currently available for other platforms. This problem is mitigated by the availability of commercial versions (existing or announced) by a number of vendors, including Intel.

The size of the cluster has proved a severe test for all the software components running on it. As shown above, our benchmarks revealed a problem within HPVM, the unsatisfactory scaling of the flow control scheme. By improving on this aspect of the design, we expect to see a further improvement in the performance scalability of bandwidth-sensitive applications like ZeusMP.

Scaling problems were not limited to HPVM, but concerned also Windows NT and LSF. For example, we discovered that by default Windows NT cannot handle more that 64 TCP connections at a time on a single socket.[4] In its first release supporting NT clusters, LSF inherited this limitation; LSF basic design, in which one remote process was managed at a time, had been extended for parallel job execution by simply iterating the startup operations over all the job's processes. During the course of two minor releases, LSF managed to fix this and other initial problems, such as a long startup time over a large number of processes and an imperfect trapping of the Ctrl-C signal in some circumstances.

From a system administration point of view, we found that Windows NT provides useful tools in some areas, such as the remote administration of services (the NT equivalent of Unix daemons), while it is lacking in others, such as remote registry access. For this and other reasons, in managing large clusters we found almost indispensable the use of disk reimaging tools.

6 Related Work

A number of projects focusing on high performance communication have produced a real prototype. Most ef-

forts involve either custom network hardware or high performance low-level messaging layers.

High Performance Communication Layers. AM (von Eicken et al., 1992) has been one of the first realizations of high performance messaging layers. The AM project started as a communication library for the CM-5 and has culminated today into the realization of a network of workstations (NOW). The NOW cluster is composed of 105 Ultra SPARC 1/170 connected with a Myricom network (Culler et al., 1997) and running the Solaris operating system. The network is a variant of the fat-tree topology, like ours. Built on top of AM, the high-level APIs available on the cluster are MPI and Fast Sockets (Rodrigues, Anderson, and Culler, 1997), a high performance version of the Berkeley Socket; MPI achieves a minimum latency of 36 μs and a peak bandwidth of 24.6 MB/s, Fast Sockets, respectively, 60 μs and 33 MB/s. A number of high performance computing benchmarks have been demonstrated (Culler et al., 1997), including the fastest disk-to-disk sorting program, and a distributed Web search engine. An implementation of Split-C has been realized that uses AM in its runtime support.

Princeton's SHRIMP project is based on two different platforms. The first uses network interfaces built as part of the project, Pentium PCs and an Intel Paragon backplane as the network switch. In the second platform, Myrinet interfaces and switches are used in place of the custom network fabric. Princeton's Virtual Memory Mapped Communication (VMMC, VMMC-2) communication software has been developed on these two platforms (Dubnicki et al., 1997). A number of small-scale clusters up to 16 nodes in size have been built. The available high-level API is an implementation of the Socket library, achieving 20 μs minimum latency and 84 MB/s peak bandwidth.

In some respects, similar to FM is the Real World Computing Partnership's PM (Tezuka, Hori, and Ishikawa, 1996). Like FM, PM runs on clusters of Myrinet-connected workstations and performs flow control and buffer management. The main difference with FM is in the optimistic flow control mechanism, and variable-sized packets. An implementation of MPI is available achieving 13 μs minimum latency and 98.8 MB/s peak bandwidth. An implementation of MPC++, a C++ with extensions for message passing has been realized employing PM for its runtime support.

Another high performance messaging layer is U-Net (von Eicken et al., 1995). Developed originally on an ATM network, it provides buffer management and demultiplexing in hardware but no flow control, and thus data can be lost due to overflow. Contrary to FM, U-Net and other messaging layers try to avoid the passage of data through kernel memory by performing a DMA transfer directly into the user buffer. The disadvantage of such a feature is that the user must declare in advance the regions of memory to be used for communication, so to allow the library to permanently pin them down.

BIP (Prylli and Tourancheau, 1997) is another messaging layer developed for the Myrinet at the Ecole Normale Superieure de Lyon. It has a higher level, more traditional message-passing interface, with both blocking and non-blocking send/receive primitives. BIP provides high bandwidth, low latency, unreliable communication, with an adaptive packet format. It has been specifically designed to support standard message-passing libraries such as MPI and PVM, for which its interface represents a good match.

Hardware Approaches. An alternative to optimizing protocol performance in software is to develop hardware that delivers performance to software by presenting the system with an interface for which it is easier to optimize the protocol stack. Hamlyn (Buzzard et al., 1996), ServerNet (Horst and Garcia, 1997), and hardware based on the new Virtual Interface Architecture standard (Compaq Computer, Intel, and Microsoft, 1997b) migrate protection checks from software to hardware, enabling user-level programs to access the network directly once the operating system has established a connection between endpoints. Similarly, Memory Channel (Gillett, 1996) and SHRIMP (Blumrich et al., 1995), each of which exports a put interface (i.e., an interface in which messages are sent to a sender-specified address on the receiver), require the operating system only to establish mappings from between nodes. All data transfers are performed user-level.

The FM interface is designed to be portable to a variety of network interfaces, including the new, nontraditional interfaces just mentioned. FM was originally implemented on the Cray T3D (Cray Research, 1993), which uses a put/get interface. It currently runs on Myrinet (Boden et al., 1995), and we are in the process of porting FM to ServerNet. In all cases, the value added by FM is in its programmability. By providing flow control and buffer management—two important features almost never implemented in hardware—FM removes the burden of delivering reliable, ordered delivery from higher-level messaging layers and applications.

7 Summary and Future Work

Leveraging on a number of readily available technologies we were able to assemble a 192-node cluster in a matter of weeks. The use of mainstream software interfaces and operating systems enabled us to quickly demonstrate a number of HPC scientific applications and to use them in the testing and evaluation phases. The cluster is currently in use as a production machine at the NCSA in Urbana.

The direct comparison using stock NCSA scientific applications demonstrates that HPVM successfully integrates a large number of PCs into a tightly coupled machine that is within a factor of 2 to 4 of SGI Origin 2000 and Cray T3E performance at a fraction of the cost. The inherent scalability of the cluster design produces a comparable, and in some applications better, speedup than the Origin 2000.

To achieve these results, we first built standard APIs (MPI, Global Arrays, Shmem) capable of delivering the performance of a high-speed interconnect to the applications (13 μs minimum latency, 84 MB/s peak bandwidth for MPI). We then provided system management services that were lacking in the NT operating system, and then we solved a number of scalability issues at different levels in the software hierarchy.

Since HPVM runs entirely in user space, it was relatively straightforward to port to NT. The appeal of NT is the affordable and extensive base of available tools, and the potential for a larger acceptance by a growing number of nontechnical users. Thanks to the integration with Platform Computing's LSF, HPVM provides robust remote job execution and cluster monitoring services.

The major scalability issue that we found came from the static nature flow control mechanism we had built in HPVM. In addition to effective short-term remedies—essentially increase in buffer space and hand tuning of critical parts of the mechanism, we are considering longer-term solutions such as a more dynamic scheme.

We believe the HPVM design to have a potential for decisive performance improvements in the future. The above changes to the flow control scheme will benefit bandwidth limited applications; we have reported a doubling of performance for the ZeusMP application when increasing the size of a critical buffer. Perhaps more important, the next generation of the Intel CPU architecture is going to have a decisive improvement in CPU floating performance, an area in which the cluster is most distant from the Cray T3E and the SGI Origin 2000.

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NOTES

1. HPVM also provides this for Linux clusters.
2. Windows is a registered trademark of Microsoft in the United States and other countries.
3. This technology is one of the contributors to emerging Virtual Interface Architecture standard from Intel/Compaq/Microsoft.
4. This limit can be removed by assigning a different value to a compiler constant in the winsock library.

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